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INTERIM DEVELOPMENT REPORT

FOR

MF RESISTOR FACTORIAL LOAD LIFE TEST

This report covers the period Jan. 1963 to April 1963

CORNING GLASS WORKS

ELECTRONIC PRODUCTS DIVISION

BRADFORD, PENNSYLVANIA

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISION

CONTRACT NO. 87385

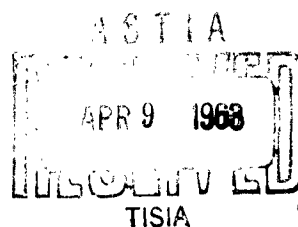
PROJECT SERIAL NO. SR008 0305 T-9601

400 288

31 March, 1963

Prepared by

Stouder C. Thompson
Stouder C. Thompson
Project Manager



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PART I

ABSTRACT

This project is concerned with performing a factorial load life test on Corning Glass Works' hermetically sealed, glass NF resistors which are qualified to Characteristic G of MIL-R-10509D. The results of this test will be in the form of detailed load life performance data. Resistors of two rated power dissipating capabilities, 1/8 watt and 1/4 watt, will be tested. In this factorial test approximately 22,000 resistors will operate at a combination of temperatures of 70°C, 100°C, 125°C, and 150°C and power dissipating levels of one time, two times, three times, four times, and five times their normally rated power for 2000 hours. In addition, 450 resistors will be tested for 10,000 hours at 70°C at their rated power.

This interim report describes activities carried on during January, February, and March 1963. Since previous reports have covered test design and earlier fabrication techniques used in assembling the test boards, this report will not repeat that information and will deal primarily with factors leading up to the completion of installation of all test component and starting of the 2000 hour test.

During this report period, the project progressed from Phase II into Phase III - Phase II having been completed. It is expected that Phase III will be complete by the end of the next report period, and in addition, a good portion of Phase IV will have been completed.

This report period consumed the major portion of work effort expended thus far. Assembling and wiring the test boards involved more man hours

PART I

of labor than all previous efforts combined. In addition, these operations proved to be the most critical from a schedule completion as well as test reliability standpoint. Therefore, a major portion of this report will deal with these factors.

Several additional modifications and additions have been made to the testing equipment; these are described in the Detail Factual Data portion of the report.

PART I

PURPOSE

The purpose of this project is to obtain failure rate data and acceleration factor data on Corning's NF glass hermetically sealed tin-oxide resistors in sufficient detail to be meaningful to U.S.Navy technical personnel and to industrial design engineers.

The project has been divided into the following phases:

Phase I

Test technique determination and equipment selection.

Phase II

- a) Equipment procurement and installation.
- b) Resistor manufacture.
- c) Start of 10,000 hour load life test.

Phase III

2000 hour load life test.

Phase IV

Data Analysis.

PART I

GENERAL FACTUAL DATA

(a) Identification of Technicians

The following is a list of personnel who worked on this project during this report period, together with their function and hours expended:

Stouder C. Thompson, Project Manager	512 hours
Robert A. Ballard, Senior Engineer	80 hours
Henry K. Gensler, Statistical Analyst	96 hours
Louis R. Stewart, Technician	512 hours
Donald I. Dunworth, Technician	20 hours
Francis J. Colella, Data Processing Technician	60 hours

(b) Measurement Procedures

Following is a list of instruments and equipment used in performing tests and measurements on the project thus far:

Temperature Measuring Equipment

1. Potentiometer, Rubicon Model No. 2746 with iron-constantan thermocouple. -55°C to 250°C in $.2^{\circ}$ steps. (1)
2. Temperature Recorder, Leeds and Northrup Speedomax G Model S 60000 series. 0 to 500°F in 5°F divisions, capable of measuring and recording at 24 points. (2)

Ovens

1. Oven, Blue M. Electric Co. Model E-SP-406 CXX 1000 watt 40°C to 250°C with Saturable reactor temperature control. (41)

PART I

GENERAL FACTUAL DATA

D.C. Power Supplies

1. E.D.Ackerman "Electus" Power Supplies Models -

6225	0 to 500 VDC	250 watts (12)
6233	0 to 24 VDC	300 watts (9)
6234	0 to 108 VDC	300 watts (3)
6235	0 to 600 VDC	300 watts (12)
6237	0 to 50 VDC	250 watts (16)
6243	24 VDC Fixed	24 Amps (11)

D.C. Voltmeters

1. D.C.Voltmeter, Weston 911 (1)

0 to 1, 3, 10, 30, 100, 300, 1000 VDC

2. Digital D.C.Voltmeter, United Systems "Digitec". (1)
0 to 1, 10, 100, 1000 VDC

3. Volt-Ohm-Milliammeter - Simpson Model 270. (1)

Digital Resistance Deviation Bridges

1. Digital Deviation Data Logger, Non Linear Systems
Model 24356. (1)

2. Digital Deviation Bridge, Non Linear Systems Model R24S. (1)

Data Processing Equipment

1. IBM Model 519 Summary Punch (2)

2. IBM Model 026 Key Punch (1)

3. IBM Model 056 Card Verifier (1)

4. IBM Model 082 Card Sorter (1)

5. IBM Model 085 Collator (1)

6. IBM Model 609 Calculator (1)

7. IBM Model 402 Accounting Machine (1)

PART I

GENERAL FACTUAL DATA

(c) Test Design

The following diagram includes all pertinent information detailing quantities of resistors to be tested. Since the last progress report, an additional group of resistors has been added to the test. These parts will be tested at two, three, four, and five times rated power at 150°C.

PARTS TO BE TESTED

NF60 SIZE (1/8 WATT)

100 ~ 1Z
1K ~ 1Z
10K ~ 1Z
100K ~ 1Z

NF65 SIZE (1/4 WATT)

100 ~ 1Z
1K ~ 1Z
10 K ~ 1Z
100K ~ 1Z
348K ~ 1Z

	PERCENT RATED OPERATING POWER				TEST TEMPERATURE (°C.)
	100	200	300	400	
TOTAL NO. PCS.					150°
NO. PCS. EA. TPE		67	13	2	2
EST. % FAILURE		2.15%	9.50%	70.0%	103%
TOTAL NO. PCS.	2340	630	270	90	125°
NO. PCS. EA. TPE	260	70	30	10	10
EST. % FAILURE	.25%	1.00%	2.50%	20.0%	
TOTAL NO. PCS.	5760	2340	1170	360	100°
NO. PCS. EA. TPE	640	260	130	40	40
EST. % FAILURE	.10%	.25%	.50%	2.00%	
TOTAL NO. PCS.	450*	3870	1980	1170	70°
NO. PCS. EA. TPE	50	430	220	130	130
EST. % FAILURE	NOT EST.	.15%	.30%	.50%	

*100 Ω & 10 K Ω NF 60 & 85 ONLY *10,000-HOUR TEST

PAGE 1

DETAIL FACTUAL DATA

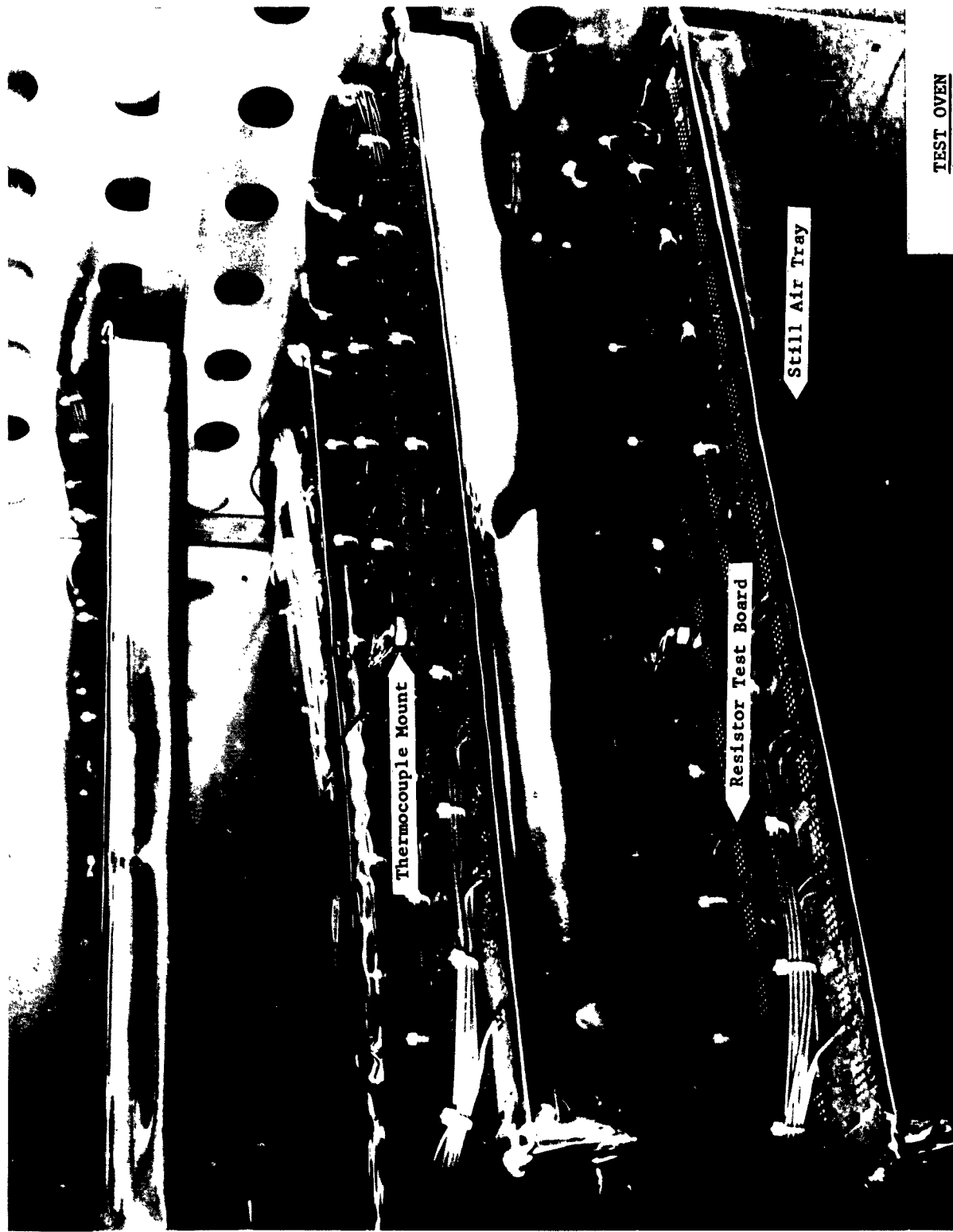
(A) Installation of Completed Test Boards in Ovens; Since the previous reports have outlined the methods used to mount parts, wire and test the individual test boards, this information will not be included in this report. The majority of effort expended during this report period was in installation of the wired test boards in the ovens and connection of the resistor power switching relays to the test board wires. A brief description of the procedure used follows:

The completed test boards with still air trays attached were placed in the oven and supported by 1/4" OD glass rods under the aluminum still air trays. The wires were then fed through the 1 3/4" diameter ports located on the rear panel of the oven. Each bundle of wires attached to a board had been marked to identify them at a later time. When all assigned boards had been placed in the oven, the wires were then segregated into groups according to sequence of assembly. Normally, plugs and relays located at the bottom portion of the chassis were wired first.

Since each test board is capable of holding 100 resistors and each plug capable of containing only 50 pins, an indexing system was developed which correlated plug, pin and wire no., to location on the resistor test board. This index was used by those performing the wiring so that a minimum of errors might be incurred.

Wires attached to the boards actually are comprised of three parts:

1. A four foot wire attached to the appropriate terminal wire on the test board and terminated at a female pin at the other end.



TEST OVEN

PART I

DETAIL FACTUAL DATA

2. An AMP 42993-2 female pin pre-cripped to the four foot wire and another 18 inch wire of the same size.
3. An 18 inch wire attached to the pin at one end; the other end prestripped and tinned for soldering to the group selector relay contact.

All wires were pre-marked and color coded for identification.

Wiring was performed in two steps:

1. The pins were inserted into the AMP 201310-1 plugs and the wire no. noted on the plug index sheet opposite the appropriate pin socket number. When all 50 pins had been inserted, the plug was inspected to assure proper assembly.
2. The individual 18" wires attached to the pins were then soldered to the relay or relays assigned to that particular plug. Before proceeding to the next plug, the operator inspected her work to assure all solder joints were of acceptable quality.

Each plug was wired and attached in this fashion until that particular chassis was completed. A full time inspector was employed to then inspect the completed chassis and read out all resistors. Discrepancies were noted on a "rework" form and the chassis re-inspected after rework operations had been performed.

Primary reasons for rework were:

1. AMP pins not properly seated in sockets.
2. Wires not properly attached to relay contacts.
3. AMP pins inserted into wrong position in plugs.

After completion of the preceding operation, the oven was considered to be ready for test commencement.



ILLUSTRATION OF OPENED CHASSIS

PART I

DETAIL FACTUAL DATA

(B) Oven Start-up Procedure

In order to distribute work effort and take advantage of a possible acceleration factor in the collection and analysis of data, resistors were put on test as soon as the test oven and switching circuits were completed, checked out, and adjusted. The procedure used for start-up is described below:

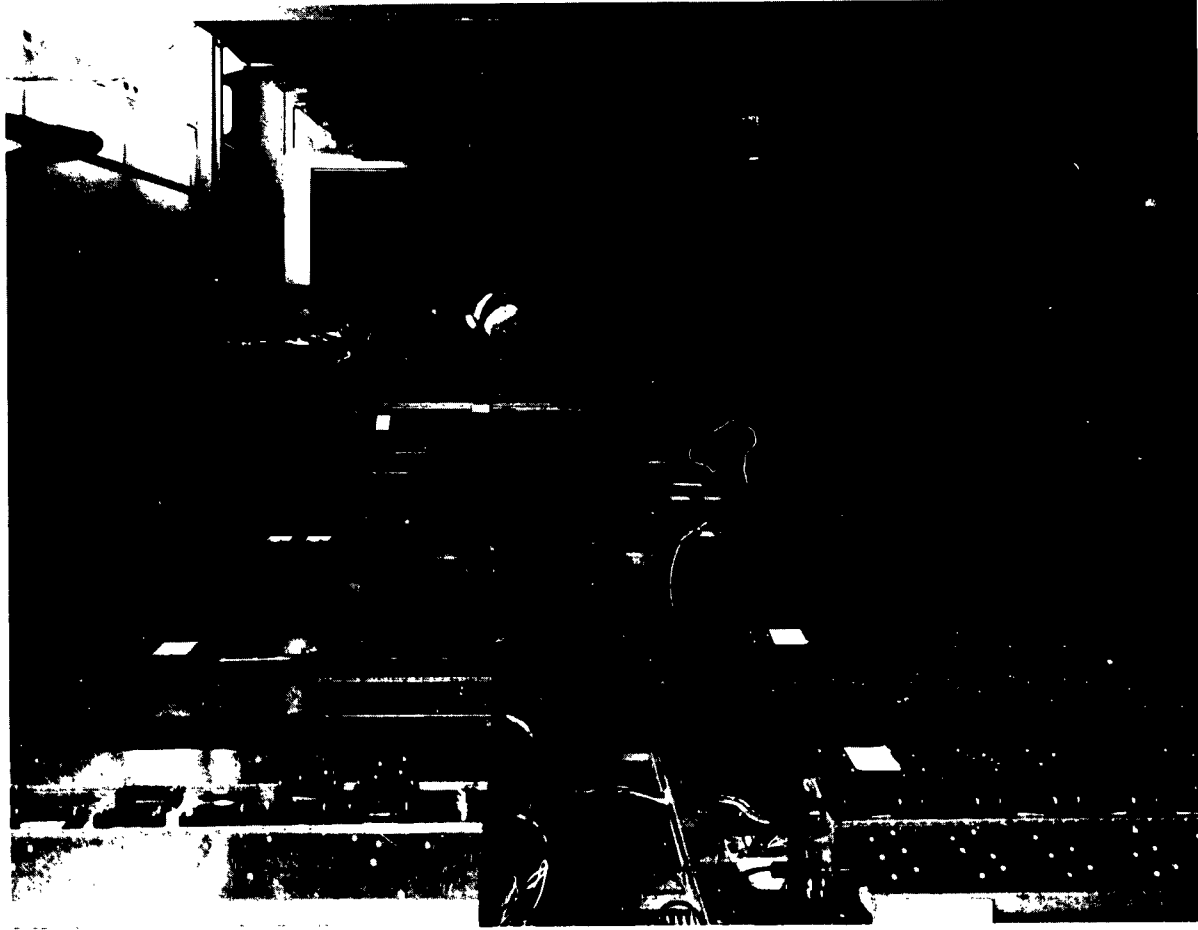
1. Prior to applying heat and voltage to the resistors, an initial resistance reading was made at $25^{\circ} \pm 5^{\circ}\text{C}$. At this time the printed tape showing initial resistance was analyzed. Any resistors indicating resistance of greater than $\pm 1\%$ of their nominal were checked at the test board to determine if a short circuit or cold solder joint may have caused excessive deviation. This was the final inspection prior to commencement of test.
2. The oven was then turned on and adjusted to nominal temperature with resistor power off. Thermocouples on all eight test boards were monitored and intake and exhaust ports adjusted for minimum temperature gradient between shelves. Maximum gradient found between any two trays was 4°C during this period. Once stabilized at operating temperature, the resistors were then read out initially and all data transferred to the computer area.
3. Resistor power was then applied and oven temperature control (R_3) adjusted so that during "power on" cycle, the average temperature of all eight trays in the oven was at specification nominal. During the "power on" cycle, the gradient between trays increased to as much as 8°C . It was found that normally the uppermost trays in the oven were the warmest and during cycling and shifted in temperature the most.

PART I

DETAIL FACTUAL DATA

In some cases, these trays would change temperature up to 7°C. By slightly shifting the tray position within the oven, it would found that this temperature shift could be minimized.

Since provisions were made to monitor temperature on one tray in each oven, the tray indicating the highest degree of shift during cycling was selected to represent the oven. Thus, it is assured that recorded temperatures are extremes for that oven and so long as the selected tray is within specification, the other trays will be too.



Photograph of Matrix Test Area showing the chassis of some of the 41 ovens installed in the area.

The operator is shown plugging the resistor measurement cable into one of the plugs on the chassis side of the oven.

This operator communicates with the NLS Digital Data Logger operator through an intercom system and provides information to co-ordinate the resistance readout; in this manner it is possible to read and record on IBM cards approximately 40 resistance measurements per minute.

(C) Description of Measurement Procedure

The procedures for measurement of resistor values have been described in part in previous reports. These procedures have been modified slightly to simplify readouts and to provide a means of cross-checking printed readout with carded data. Readout procedure consists of:

1. Standardization
2. Stabilization
3. Readout
4. Data Check
5. Rapid Data Analysis

Standardization

As described in the previous report, a resistance standard was fabricated so that rapid standardization of the Digital Data Logging system might be effected each time prior to readout. The standard consists of 50 resistors encapsulated in RTV silastic coated with epoxy resin and attached to a plug which mates with the readout cable plug. The standard is read out each week with an L&N Model 4735 Wheatstone Bridge. These values are posted on a standardization chart and compared against previous readings. Prior to each oven readout, the standard is read and resultant values posted against standardized values. Throughout the use of the NLS 24356 Digital Data Logger, a stability factor of $\pm .04\%$ has been observed.

Standardization in this manner thus assures that the measurement equipment is operating satisfactorily.

Stabilization

When a resistance readout is to be made, the operator sets up the master power control panel. This is accomplished through a series of interlocks so that the test cannot be accidentally interrupted. Once the panel has been set up, the power cycle continues until the resistor power is automatically shut off. A timed cycle then occurs which allows the resistor temperature to stabilize. At the end of the stabilization period, a buzzer sounds and indicator lamp lights. This indicates to the operator that the resistors are ready to be measured. When readout has been completed, the interlocks are again activated and the power cycling resumes.

Readout

Resistance readout is performed by two persons; a test room operator and data logger operator. Since the data logging equipment is located some 50 feet from the test area, the operators communicate thru an intercom system. The test room operator provides information to the data logger operator so that the readout may be co-ordinated and completed in minimum time. The test area operator provides information as to what plug is being measured, how many resistors are terminated there and when the plug-in is completed. In addition, the readout operator provides immediate information to a technician standing by so that any possible errors or apparent resistor failures may be checked immediately. Any failures not directly associated with the resistor itself are repaired and the test piece re-read before testing progresses further. If a resistor has failed, this information is noted on the data logger operator's log sheet and at the next readout this information is available.

Data Check

After the resistors readout is completed, the data logger operator checks the printed tape data against the carded data. In addition, the carded data is scanned to detect any possible discrepancies in the recording of fixed identification data. If all data thus checked is found to be without error, the carded data is marked indicating that it is in order. The printed tapes are then given to the statistical analyst who retains them until all carded data is analyzed.

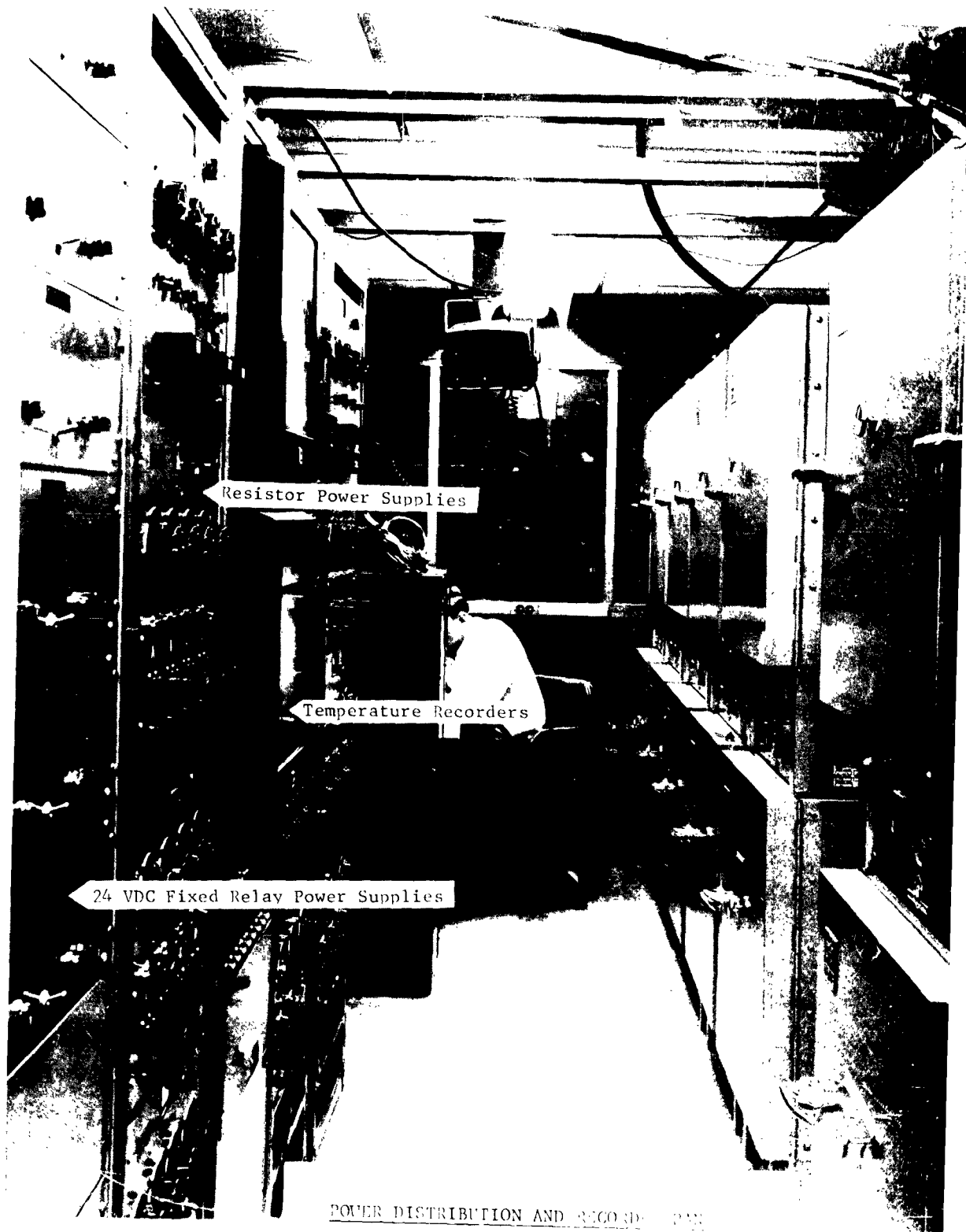
Rapid Data Analysis

Because it is important to know if the test resistors are behaving abnormally within a short time after they have been read out, a system for rapid data analysis has been devised. If test resistors seem to be behaving abnormally, test equipment must be checked thoroughly and if apparent, malfunctions corrected prior to continuing the test. Since visually scanning all data cannot be performed in a short time, an IBM 082 card sorter is employed to detect abnormalities.

Immediately after readout and data check, the carded data is transferred to the computer area. The cards are quickly sorted in orders of ascending resistance changes (ΔR). Cards which fall outside of limits for the group are then scanned to determine what extremes or what quantities are involved. If these values indicate something other than what is expected, the statistical analyst immediately notifies the test area technician and the testing equipment is thoroughly examined for possible malfunction.

Data is then accumulated until all test ovens have reached the first specified readout interval. The individual carded data is then transferred to a "Life Summary Card" which will contain all periodic readings. As all ovens pass the specified readout intervals, the Life Summary Cards

are tabulated and printed. This early data tabulation will enable the statistical analyst to determine a good portion of the summary data prior to termination of the test.



(D) Circuit Modifications

During the report period, several additional circuit modifications were made. They are explained below.

Master Timing Control Circuit

Prior to starting the first test oven, all power supplies, ovens, and switching circuits were tested. It was found that the power supplies would not supply a constant voltage under varying loads. Although this was known prior to purchasing the supplies, the degree of variation was not known. In testing the voltage output from minimum to maximum load capabilities, it was found that the voltage decreased approximately 15% as the load was increased from minimum to maximum. This made the original plan of having each group of resistors in an oven operate independently of other groups unfeasible. Further experimentation indicated that two options were possible. 1. Regulate voltage for all supplies. 2. Apply power to all groups of resistors simultaneously. In studying the two options, the first was readily eliminated for several reasons, primarily cost. The second option offered several advantages in addition to being relatively simple to effect. Advantages are:

1. All ovens are operating in parallel cycles. Thus, all tray temperatures, power supply voltages, and loading conditions are relatively the same for any given time interval. This mode of operation makes it easy to detect any malfunction or drift condition since all oven and tray temperatures are recorded and appear as a group in a straight line on the recorder chart
2. Voltages remain stable throughout power cycling since there is a constant load on the power supplies

3. Adjustments may be made at any time to any oven without affecting other test ovens.
4. The counter on the master time control provides an additional record of how many two-hour cycles have occurred and any period of time may be related to this record. Thus, in a 24-hour period, the counter will record 12 counts and the accumulated counts provide a cross check against scheduled run time.

Temperature Alarm Circuit

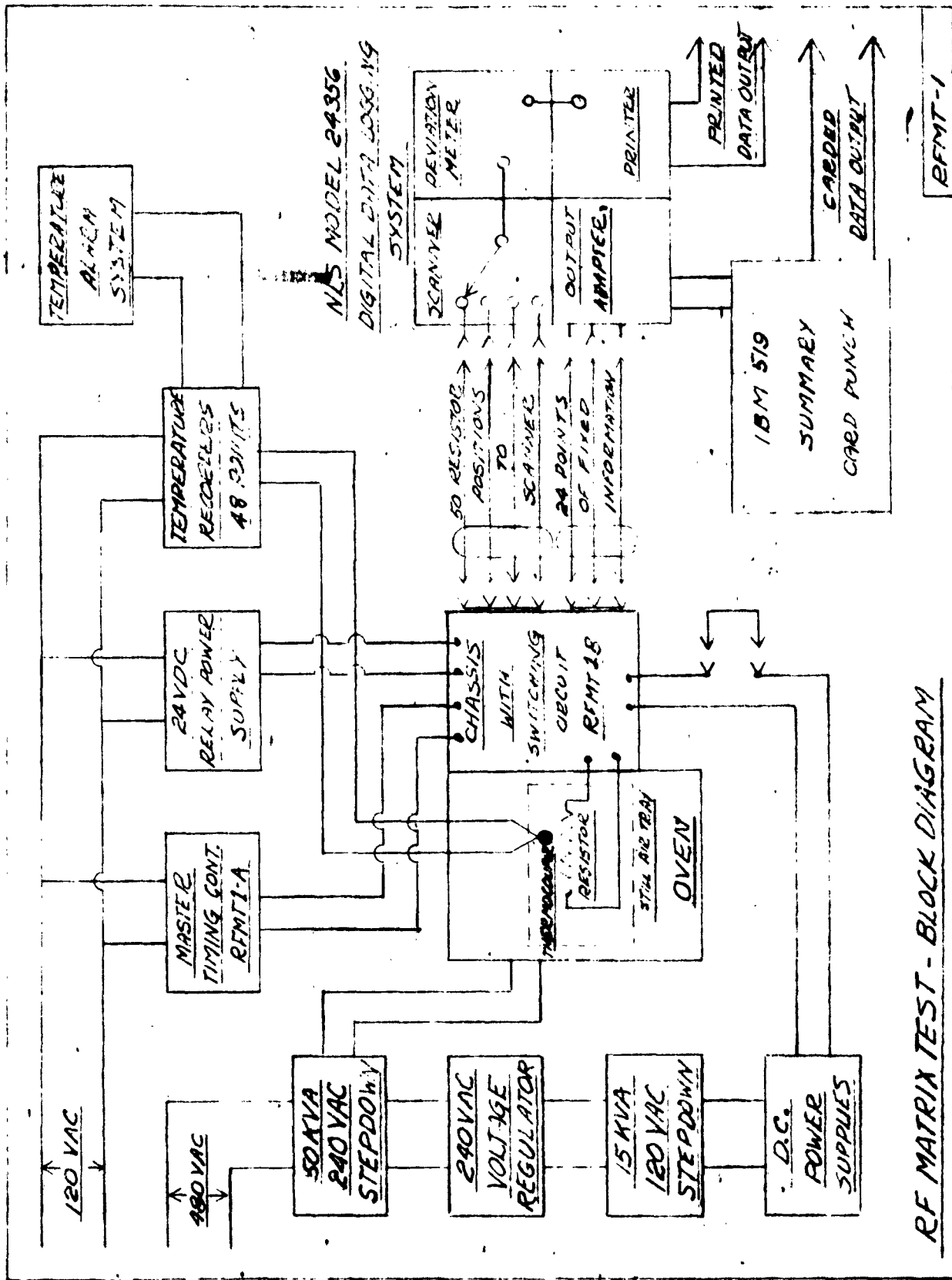
A temperature alarm has been added to the 24 point recorders so that minimum and maximum limits may be set for each recorded point. Each recorder is capable of triggering an alarm if preset limits are exceeded for either one of two recorded temperatures. The alarm provides an audible as well as visual alarm and, in addition, will sound an alarm in an adjoining test area if limits are exceeded.

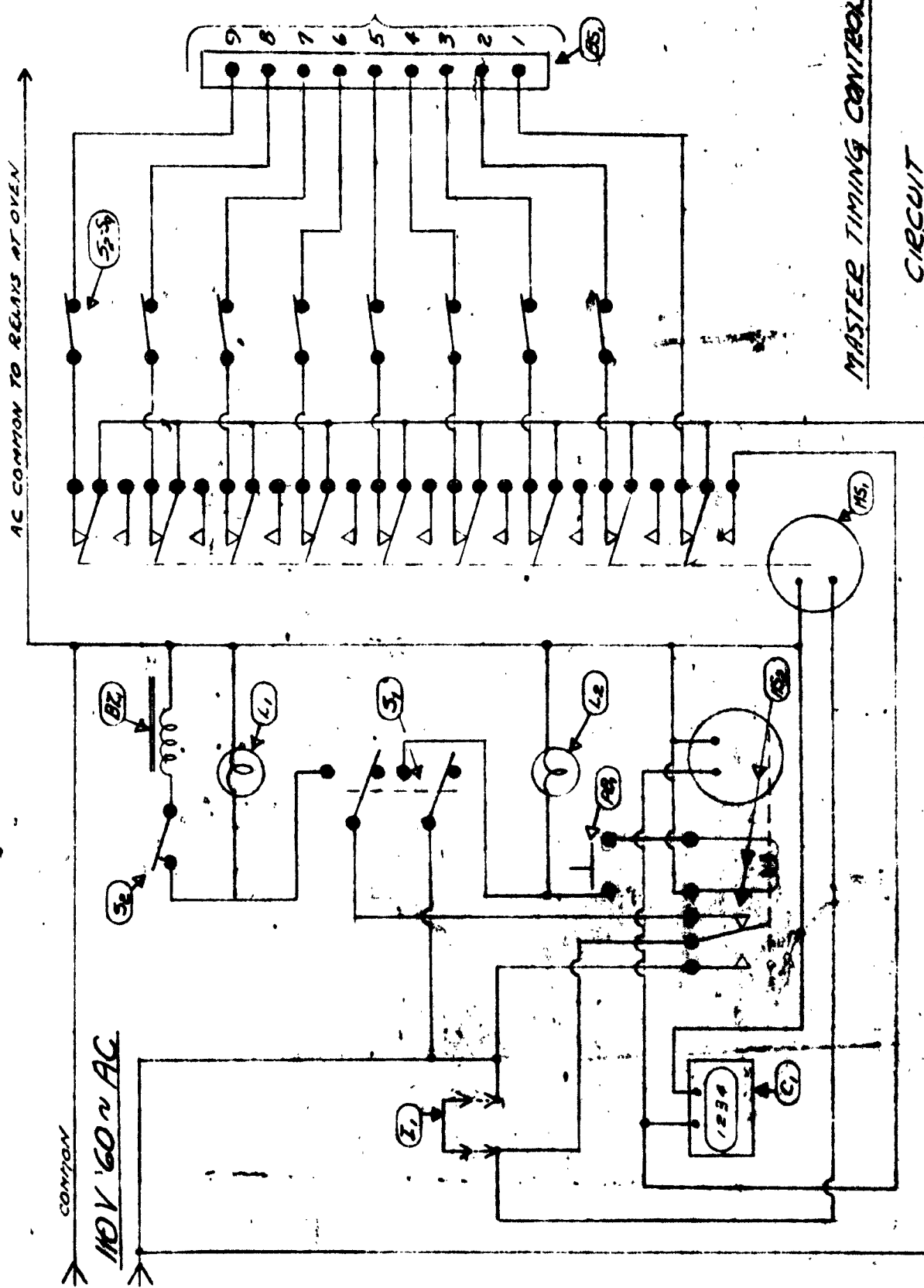
Alarm points are set as follows:

- 70°C nominal-alarm sounds at: 60° or less - 80° or more
- 100°C nominal-alarm sounds at: 90° or less - 110° or more
- 125°C nominal-alarm sounds at: 115° or less - 135° or more
- 150°C nominal-alarm sounds at: 140° or less - 160° or more

An emergency action procedure has been provided in case the alarm should sound. This procedure contains all information necessary to correct the conditions which may cause temperatures to vary beyond specification or alarm limits.

The following block diagrams and schematic drawings reflect the final circuit arrangement.





Circuit

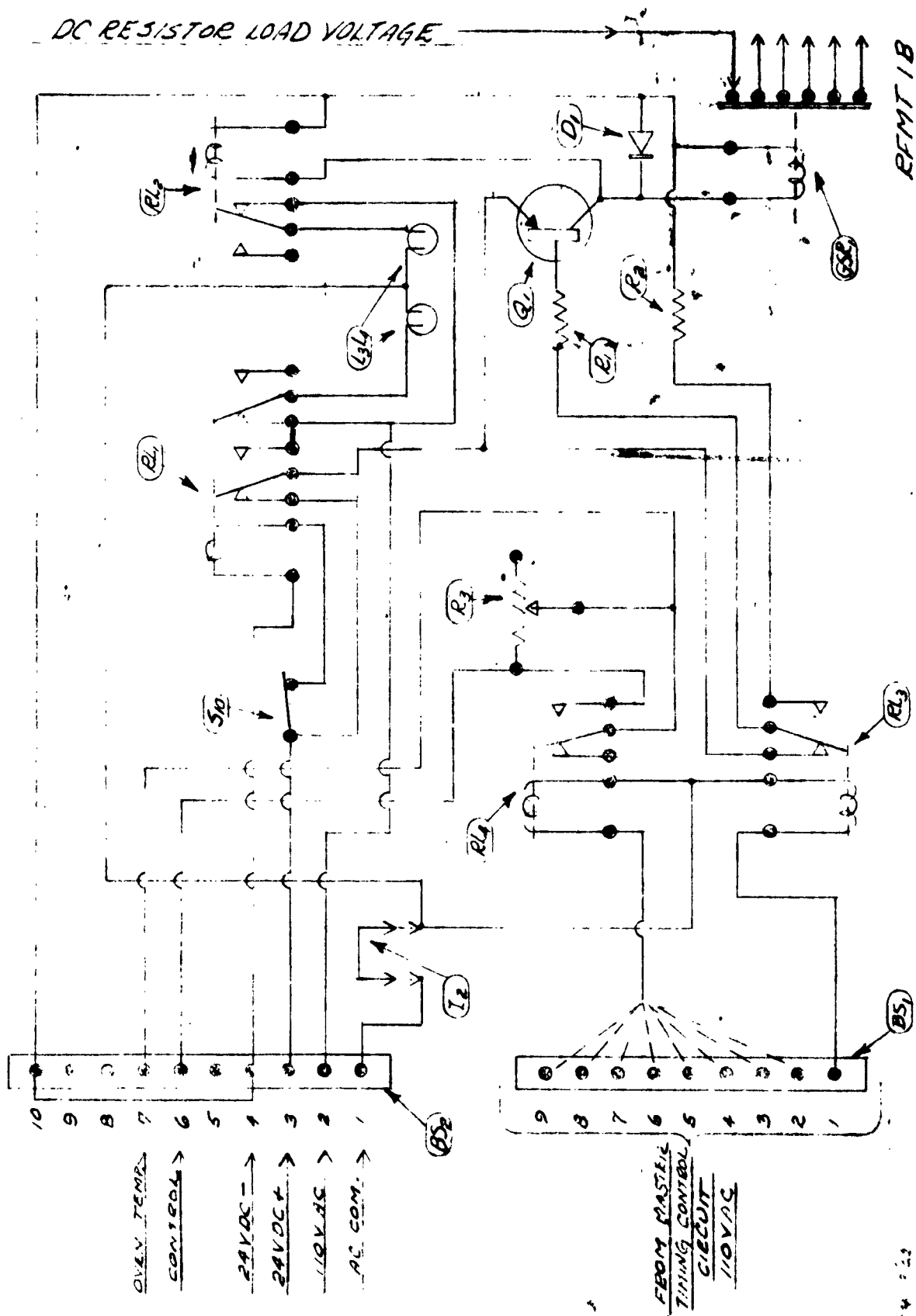
CRM 11

PARTS INDEX

MASTER TIMING CONTROL CIRCUIT RFMT1A

<u>SYMBOL</u>	<u>QUANTITY</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER</u>	<u>NO.</u>
MS ₁	1	9 Ckt.Time Switch	Ind.Timer Corp.	MC-8-A-24-10
MS ₂	1	Single Cycle Time Sw.	" " "	RC-5-A20-1
S ₁ -S ₉	9	DPDT Switch	Carling	2GL-5373
BZ ₁	1	110 VAC Buzzer	Guardian	BU-115
L ₁ -L ₂	2	Indicator Lamp 110V	Dialco	G431
PB ₁	1	Pushbutton Switch	Carling	FA-754
C ₁	1	Counter	Gen.Controls	CZ600AS602
I ₁	1	Interlock Jack	Gen.Radio	274-MB
BS ₁	1	Barrier Strip	Cinch Jones	10-142

RESISTOR LOAD VOLTAGE SWITCHING CIRCUIT



PART I

CONCLUSION

During the report period, Phase II was completed and approximately 25% of Phase III completed.

All operations involving assembly of test components were completed and no serious problems or schedule delays were encountered.

The test circuitry was altered once again and is now operating satisfactorily. The modifications simplify circuit operation and provide a ready means for detection of circuit malfunction, should it occur.

All test ovens have been started and up to 1000 hours of test time have accumulated on some resistors.

The 10,000 hour test has logged approximately 2500 hours and all components are behaving normally.

In general, no significant schedule delays have been incurred. The following project performance and schedule chart indicates status for all phases of the project.

PROJECT PERFORMANCE AND SCHEDULE FOR
PROJECT SERIAL NO. SR008 035 T-9601

CONTRACT NO. NOB sr 87385

MARCH 31, 1963

LEGEND:

PERIOD COVERED: 1/1/63 to 3/31/63

WORK PERFORMED

SCHEDULE OF PROJECTED OPERATIONS

1. TEST DESIGN & PROCUREMENT

Test Design

Equipment Design

Equipment Procurement

2. COMPONENT MFG. & SCREENING

Mfg. Resistors

Screen Registers

3. ASSEMBLY OF RESISTOR BOARDS

Mount Resistors on Boards

Wire Boards

Assembly Box

4. INSTALLATION OF EQUIPMENT

Oven Installation

Power Supply Installation

Resistor Board Installation

5. LOAD LIFE TESTING

10,000 Hr. Test

10,000 Hr. Test

6. DATA PRESENTATION

10,000 Hr. Test Data

2,000 Hr. Test Data

ESTIMATED COMPLETION in percent of TOTAL EFFORT expected to be expended.

1. TEST DESIGN & PROCUREMENT

2. COMPONENT MFG. & SCREENING

3. ASSEMBLY OF RESISTOR BOARDS

4. INSTALLATION OF EQUIPMENT

3. LOAD LIFE TESTING

6. DATA PRESENTATION

100%

100%

100%

100%

322

107

PART II

PROGRAM FOR NEXT QUARTER

During the next quarter April through June 1963, the following tasks are scheduled:

- 1. Complete Phase III of this project. IE, complete the 2000 hour load life test.**
- 2. Assemble all data for presentation and determination of acceleration factors and development of the High Reliability specification referenced as Item 1 of this contract. It is hoped that the major portion of this information will be available by the end of the referenced report period.**
- 3. Complete analysis of all failed parts for failure mode categorization.**
- 4. Continue to collect data re the 10,000 hour test.**